AUSTIN SILICON INCORPORATED
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Company Resume

Austin

OBJECTIVE:

To provide quality short and long term consulting services for the following VLSI related projects:

Circuit Design:
• Full Custom Circuit Design For Digital and Mixed Signal Platforms
• Design, Development and Testing Of Low Power and High Power IO, Padring and ESD circuits
• Library Development, including layout supervision
• Testing, Migration and Characterization of Existing Designs
• New Process Evaluation
• Full Project Management
• Training – Design, Simulation and Debug

Logic Design, Test and Related Engineering Development:
• Logic Synthesis For Control Units Using Cadence-Synopsis and Other Packages
• Custom Logic For ALU, MMU and Others
• Verilog, VHDL and Other Simulation Tools
• Overall Project Management
• Impart Training To Individuals

Layout Design, Place and Route, Floor Planning:
• Custom, Synthesized and Migrated platforms Design
• Training – Instruction, Monitoring and Review

EXPERIENCE AND TRAINING:

We at AUSTIN SILICON, INC. take great pride in the employees we send to the customer job site to represent our company. Each engineer brings with him many years of industry experience and familiarity with the latest tools. Training on circuits and other aspects of design are imparted by qualified engineers on a need basis.

Back to top

CLIENT HISTORY (Example):

Advanced Micro Devices
Mathstar Corporation
Silicon Metrics Corporation
Intel
Coherent Logix Incorporated
Intrinsity Incorporated
Coinlab

Coinlab November 2012 through April 2013
Scientific devices company. They are headquartered in Seattle.

Services Provided:

• Designed padring, clock module, and datapath design

Intrinsity Incorporated January 2007 through February 2008

Intrinsity is known for its unique FAST14 solution to high speed integrated solutions. They are headquartered in Austin.

Services Provided:

• Designed a Jtag TAP controller with interfaces for 2.5 Ghz Memory Bist and OnChipDebug. Delivered verilog RTL, synthesis deck, complete floorplan in 90nm with power grid, and Pathmill analysis. The Magma Blastfusion tools were used for all deliverables.

• Designed 2GHz 64 bit Timer, 32 bit Decrementer and Timebase unit in TSMC 90nM process. Delivered RTL, STA and Floorplan.
• Developed synthesis ready 2.5 Ghz custom cell library (Magma Volcano) for 65Nm TSMC process.
• General stdcell library support for various technologies.

Intel (Chandler) 2006

Intel is the pre-eminent chipmaker in the world and does not need an introduction.

Services Provided:

> • Migrated the Xscale core named Manzano from 130nm to 65nm which included the following work:
> • Circuit fixes related to signal edge rates, speed paths, signal integrity.
> • Logic equivalency tests using LEC and architectural verification runs using Intel's own pattern matching tools.
> • Pathmill timing analysis tool was used to analyze and fix problems with domino and other non-standard designs.
> • Layout changes were verified both visually and using erc and lvs.
> • All tasks were completed and delivered in a timely manner.

Coherent Logix 2005 through 2006 – Circuits and Verification

Coherent Logix is a small company in Austin. They do defense related designs and their principal customer is the DoD.

Services Provided:

• Full chip schematic timing analysis, synthesis methodology, IO/ESD designs, Power Management architecture and C4 bumps based Padring layout supervision of the HyperX processor. This is a large network based arrayed processor containing 15M transistors meant for Hyper Spectral applications.
• Full chip timing analysis on an extracted netlist customized for this purpose. The analysis was carried out using Cadence's RC and FE (First Encounter) tools.
• Developed RC synthesis scripts for the team. The script has been successfully used to synthesize varied designs within the chip and uses methods to ensure proper interface timing between the arrayed processors. Both Synopsis and Cadence's tools can use the scripts.
• Assisted with full chip gate simulation efforts using Modelsim and Debussy.
• Designed a 1.8v EIA-644 LVDS IO driver and differential receiver with a low power shutdown mode. The receiver has 100mv sensitivity over the entire 1.8v range. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. The Padring is capable of being switched off in sections with an external or software Wakeup feature. Designed the driver for the 1.8v SSTL_18 outputs.

Advanced Micro Devices 2003-2004, 2012

AMD is a well-known desktop chipmaker with popular products such as Athlon and the K5 processors. We consulted with the Opteron design team in Boston and Austin to help develop the latest pcix2 specification hyper transport IO for production. This is the version 2.0 of the pcix specification intended to run at 533 mbit data rate. Initial tests reveal that the part is functional at 533 mbit/s, this the first time this performance has been achieved in the industry.

Services provided:

> • Provided backend support namely timing driven place and route, clock tree synthesis, primetime analysis and custom library cell development for high speed clocks.
> • Tested the design for 133, 266 and 533 Mbit/s compliance and wrote a report. The job was to help with design and debug of the IO cell and testing the output buffer and input buffer for spec compliance. Other efforts were applied in evaluating the package limitation at 533 mbits and identifying high current modes during sleep state.

- Delivered .LIB timing files. The job included writing the .lib files for global timing and place and route tools. Hspice analysis of arc's relating to core-to-core and core-to-pad signals were determined.

MathStar Corporation 2002 through 2003

Mathstar Corp. is based in Minneapolis, Minn. They are an up-and-coming company breaking ground with their proprietary FPOA's (Field Programmable Object Arrays) and DSP parts designed in 130nm TSMC process. We consulted for MathStar via a contract through North Shore Circuit Design based in Austin, TX.

Services Provided:

- The job was to design a unique 1Ghz Field Programmable Object Array that was hexagonal in shape to allow a 6-way communication between independent processor/neighbors. The part had networking application and following work was done during the design phase:
- Modeling of the architecture to confirm 1Ghz speed. This included modeling the critical datapath to latch and forwarding to the worst-case neighbor within a specified amount of time.
- Designed and tested library components for 1GHz operation. This included designing the cells, writing verilog description and testing gate and behavioral models.
- Clock design and routing for the whole chip.
- Layout of the interconnected processors floor plan, Metal Plan and Chip Plan.

Silicon Metrics Corporation (Magma Design) 2002

Silicon Metrics now Magma Design is a well-known EDA company known for the groundbreaking SiliconSmart ™ Tools including CellRater, MemRater and IORater. Their clients include Intel, AMD and other well-known chip companies. We helped design their flagship product the IORater. This product allows a company to characterize any kind of IO cell with canned or custom IO specs. The product is capable of compliance testing LVDS, USB1.0, USB1.1, I^2C, I^2S, SDRAM Interface, and other designs. The products has had good reviews and made the cover of Electronic Design Magazine in August 2002.

Austin Silicon Incorporated directed and/or developed almost all aspects of the IORater product.

- Product Definition and Architecture for the IORater: This included defining the tool suite for licensing purposes. The functional architecture of the product that defined in detail how various components of the product would interface with each other. For example it indicated how many different types of input, scratch and output files would be needed for each published specification. And how the tool would decipher each specification.
- Details of the spice stimuli needed for each specification and circuit modeling of the harness needed to model the chip external and Internal worlds. The harness for example represents resistors tied to supplies for IOH and IOL current tests.
- Specifics of signal measurements needed to verify compliance to the specifications.
- Presentation of the compliance and error reports with graphical display of the failures.
- Help with technical publications.
- Identification of target group for marketing purposes.
- Customer visits, and EIA certification.

REFERENCES:

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Education:
MSEE, University Of Texas At Austin
MSc. Atomic And Molecular Physics, University Of Karachi
BSc. Physics, University Of Karachi

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Objective

Frontend-Backend (RTL-GDSII), Power Rails Design, custom ASIC circuits, IO/ESD/Padring design.

Profile

Lead Application Engineer supporting frontend tools and Voltus rail analysis. Worked on backend design of lntel's one teraflop Knight's Corner (KNC) processor and the Haswell processor. Previously worked on intel's 8 Ghz Tejas circuits. Low power DSP chips. Patents awarded in Mixed Signal IO designs. Experienced in CPF/UPF Powerintent based Low Power designs. Familiar with Cadence, Synopsis and Magma digital tools. Engineering consultant for 6 years. Proprietary design of PCIX 2.0 32 bit IO performing at 533 Mb/s spec.

Core competencies include: RTL compiler (RC), floor-planning, timing driven Place and Route (PR/PNR), physical synthesis, clock tree synthesis (CTS), clock mesh design (CTM), Design compiler (DCT), Physical compiler (ICC), Conformal tools Verplex/LEC Logical Equivalency Checker, Primetime (PT/STA), Cadence Power Format (CPF), Universal Power Format (UPF IEEE 1801). Voltus Power Integrity, Array circuits Spice modelling, library cell development, custom asic, IO circuits (usb, i2c, ddr, lvds, sstl, lvttl), Pathmill, Jtag design, LVS, ERC, DRC, electromigration/IR drop (EM/IR), Signal Integrity (SI), layout extraction, Modelsim, Debussy, Hspice, Spectre.

Professional Experience

(2013-Present)   (Cadence Design Systems. Austin, TX)
Lead Application Engineer

- *AE lead for Synthesis (RC Compiler), Formal Equivalence (Verplex/LEC), Conformal Low Power (CLP), Common Power Format (CPF), IEEE 1801 UPF, Voltus Power Integrity Solution.*

(2012-2013)   (Austin Silicon Incorporated. Austin, TX)
Design Engineering Consultant

- *Coinlab Inc., Seattle, WA (2013-)*: *Completed* IO and Padring circuit design for 2Ghz data transfer in 65nm SMIC process. Worked on physical synthesis of core and laid down the groundwork for floorplanning and Placement using Silvaco backend tool suite.

- *Advanced Micro Devices, Austin, TX (2012-2012)*: Integration of Kryptos testchip. Work included PNR, clock-tree synthesis, floor-planning, STA of lib cells and io signals, EM/IR analysis and custom clock macros development.

(2008-2012)   (Intel Corporation. Hillsboro, OR)
Analog Integration Engineer: Many Integrated Core(MIC) Design, Digital Enterprise Group (DEG)

- Worked on low power version of the Haswell (HSW) processor designed for throughput computing. Recently completed design of the 1 terraflop Knights Corner (KNC) processor. KNC is the newly released 50+ core processor based on the new 22nm 1.6 Ghz Tri-Gate (Finfet) process. This process is characterized by low leakage at low Vt and high voltage. It has a phenomenal high frequency performance at low voltage. HSW uses a low voltage/power version of this process meant for next version of Macbook Air with 16 hours battery time.
- HSW -- Worked on 3 latch/flop based synthesis blocks. Responsible for frontend and backend timing/critical-paths/CTM/power/DFM design. LEC and fullchip timing fixes. Provided solution from DCT to metal fill.
- KNC -- Completed backend integration (floor-planning to metal fill) of 3 top level analog/digital *Megablocks* namely *LDIO, LDIOPLL and LPCPLL*. The first is an IO block and the others are analog PLL's. Managed block/chip level static timing analysis (STA) using Synopsis DC and ICC tools. Used frontend/physical Universal Power Format (UPF) based synthesis to do signal and power floor-planning of 5 local and top level supplies. Completed CTS of 1.6 Ghz core clock and 100 Mhz test clocks routes. Manually pre-routed critical clocks. Completed LEC and fullchip noise analysis.
- UPF Low Power Design -- Pioneered Synopsis's Power Aware UPF and Powerintent based tools to place and route an IO and PLL blocks with embedded regulators. This allowed RTL to be free of all power definitions.

It also eliminated manual level-shifter insertion between power domains by auto placing them. Five power domains including regulated and switched ones were automatically floor-planned by this method.

(2001-2008)   (Austin Silicon Incorporated. Austin, TX)
Design Engineering Consultant

- *Intrinsity Incorporated. Austin, TX (2007-2008)*: Designed a TSMC 90nm Jtag TAP Controller, MBIST Jtag interface, On Chip Debug (ocd) Jtag 2.5 Ghz interface, 2 GHz 64 bit timer, 32 bit Decrementer and Timebase unit. Delivered RTL, Synthesis, Floorplan, and Pathmill timing analysis. Used Magma BlastFusion tools.

- Created 2.5 Ghz standard cell library Volcanos using Magma. These components were designed with custom cells that replaced slow blocks in the ARM core. Completed power domain analysis of the revised ARM core.

- *Intel Corporation. Chandler, AZ (2006-2006)*: Migrated the Xscale core Manzano from 130nm to 65nm. Fixed edge rates, speed paths, SI, LEC, architectural verification using Intel's pattern matching tools. Pathmill timing analysis of domino designs. Completed ERC and LVS.

- *Coherent Logix. Austin, TX (2005-2006)*: Completed full chip timing analysis, gate sim, synthesis setup, area array C4 IO/ESD designs, power management unit and padring of the HyperX processor. This is an arrayed processor containing 15M transistors meant for Hyper Spectral applications. Tools used were Cadence RC, FE, Modelsim and Debussy.

- Designed a 1.8v EIA-644 LVDS IO driver and differential receiver with a low power shutdown mode. The receiver has 100mv sensitivity over the entire 1.8v CMR. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. The Padring is capable of being switched off in sections with an external or software Wakeup feature. Designed the pad driver for the 1.8v SSTL_18 outputs.

- *Advanced Micro Devices. Austin, TX (2004-2004)*: Designed a pcix2.0 533 mbits/s IO. This IO is one of a kind and handles all pcix specs namely 33, 66, 133, 266 and 533 mbits/s. PrimeTime, Starsim simulations of all 64 IO bits. Delivered Technical Analysis Report. Part is used in Opteron interfaced to a hyper transport bus.

- Designed the above cell using proprietary slew rate control using 130nm UMC process with 1.2V supply for core and 3.3V and 1.5V for the output buffers (mode 1 and 2 respectively). This is a non-analog design so it is easily scalable.

- **Patent** (in progress): Process Switchable Low Noise Output Buffer.

- *Mathstar Incorporated. Dallas, TX (2003-2003)*: Designed clock-tree, speed-path circuits and library cells for a 1Ghz networking chip called the Field Programmable Object Array Processor. Design uses hex shaped processors array for 6-way communication.

- *Silicon Metrics/Magma Design. Austin, TX (2002-2002)*: Designed the EDA tool SiliconSmartIO. This was a flagship product used to certify and design specialized as well as standard IO's. The tool also does Padring analysis and offers insight into design flaws. The capability includes compliance testing LVDS, USB, I2C, I2S and SDRAM Interface by using Spice analysis customized for each specification. The product was on the cover of Electronic Design. Deliverables included: a) A textual description of modeling issues implied by the specs b) Spice decks for each model c) Methods of signal measurements to verify compliance to published specs d) Interface to the EDA tool SiliconSmart Cellrator used to generate static timing files and .LIB e) Graphical display of compliance f) Help with technical publications and press release g) Product licensing, h) Customer support, and EIA certification.

(1998-2001)   (Intel Corporation. Austin, TX)
Design Engineer: StrongArm, Xscale, Tejas Desktop Platform Group (DPG)

- Developed 7GHz library cells in 2 aspect ratios for DPG's 64bit processor Tejas. Completed Low Noise 50ps CK-Q FF, CSA, Fast 72 bit adders, 30ps Zero Detects. Delivered Verilog model, Static Timing analysis, .LIB, Noise Analysis tests.

- Floor-planned the ARM Core and power management module. Designed ESD, Padring, USB and a Low Noise Programmable IO buffer for the low power 600 MHz, 0.25W Xscale part called Cotulla. Created Pad-Package mapping, designed Package Substrate, Package Pinorder, tests for 0.25W operation and tests for 75uA Sleep and Drowsy Modes. These modes along with Power Island circuits were   innovations for low power. Verified design by modeling and simulating 256 pad cells in VHDL, wrote test fixture for the Padring, hand created .LIB files for IO Cells including analog ones, ran STA on extracted Padring. Created IBIS models for the drivers as well as board models for various applications.

- Designed the SDRAM memory interface IO buffers for the low power 0.5 Watt StrongArm SA1110. The design incorporates a Sleep Mode that switches off some supplies to core and Padring under Powersave conditions. Wrote Verilog models for the IO cells and Jtag and ran Regression tests. Developed and modeled design rules for boards and created IBIS models. Attended training for Synopsis Black-Box Timing Model.

- **Patents**: A Low Leakage Level Translator, USB Cable Disconnect Detect, Driver Z-Match output buffer, Regulator Independent IO Sleep Controller.

- **Award:** Leaping Lizard Award For Excellent Contribution.

Previous Tenures: Motorola Incorporated. **Defensive Publication:** Preventing False Latching In VLSI Circuits.
Advanced Micro Devices. **Patent Accepted:** A Supply Bounce Controlled Output Buffer.

Education

MSEE	University Of Texas at Austin	Austin, TX
MSc (Atomic and Molecular Physics)	University Of Karachi	Karachi, Pakistan
BSc (Physics)	University Of Karachi	Karachi, Pakistan

Interests

Power Aware methods (UPF/CPF) and Low Power design

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