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Zahid Ahsanullah

Objective

Seeking a challenging design position that requires detailed knowledge of physical design as well as transistor level analog design. Projects requiring AoT and DoT expertise would be ideal.

Profile

Design engineer experienced in large microcontrollers and small dsp chips. Application Engineer supporting Voltus and Voltus-Fi Rail Analysis tool on CPF/UPF based 16nm designs. Voltus/Fi Powergrid Views (PGV) and EMIR integrity. Expert author of application notes and rapid adoption kits. Comfortable with both analog and digital tools. Previously an application engineer for frontend-backend and conformal tools. Worked rtl-gdsii flow on Intel's one teraflop Knight's Corner (KNC) processor and the Haswell processor. Circuit engineer on intel's 8 Ghz Tejas chip and low power DSP chips. Patents on Mixed Signal IO circuits.

Core competencies include: Voltus Power Integrity, VoltusFi transistor level macro modeler for AoT designs, RTL Compiler (RC), floor-planning, timing driven Place and Route (PR/PNR), clock tree synthesis (CTS), clock mesh design (CTM), Design compiler (DCT), Physical compiler (ICC), Conformal tools Verplex/LEC Logical Equivalency Checker, Primetime (PT/STA), Cadence Power Format (CPF), Universal Power Format (UPF IEEE 1801). Array circuits Spice modelling, library cell development, custom asic, IO circuits (usb, i2c, ddr, lvds, sstl, lvttl), Pathmill, Jtag design, LVS, ERC, DRC, electromigration/IR drop (EM/IR), Signal Integrity (SI), layout extraction, Modelsim, Debussy, Hspice, Spectre, AMS and Virtuoso flows.

Professional Experience

Cadence Design Systems. Plano, TX   2013-Present
Lead Application Engineer

- Voltus and VoltusFi support for 7 leading edge customers. Previously supported Synthesis (RC Compiler), Formal Equivalence (Verplex/LEC), Conformal Low Power (CLP), Common Power Format (CPF), IEEE 1801 UPF. Support for 28nm-16nm design. Also supports 130nm and older technologies. Author of several Application notes including Electromigration, ESD and CPF. Expert in Rapid Adoption Kits design and customer testcase development.

Consultant. Austin Silicon, Austin, TX   2012-2013
Design Engineering

- *Coinlab Inc.*, *Seattle*, *WA*: Completed I/O and Padring circuit design for 2Ghz data transfer in 65nm SMIC process. Worked on physical synthesis of core and laid down the groundwork for floorplanning and Placement using Silvaco backend tool suite.

- *Advanced Micro Devices*, *Austin*, *TX*: Integration of Kryptos testchip. PnR, clock-tree synthesis, floor-planning, STA of lib cells and io's, EM/IR analysis, custom clock macros.

Intel Corporation. Hillsboro, OR   2008-2012
Analog Integration Engineer: Digital Enterprise Group (DEG) Many Integrated Core (MIC)

- Throughput computing design of the 1 terraflop Knights Corner (KNC) processor. KNC is a 50+ core processor based on 22nm 1.6 Ghz Tri-Gate (Finfet) process. The process is characterized by low leakage at low Vt and high voltage. Offers phenomenal high frequency performance at low voltage. Haswell (HSW) is the low voltage version designed for Macbook Air offering 16 hours battery time.
- HSW -- Rtl-GdsII-metalfill on 3 latch/flop based synthesis blocks. Analyzed block timing, critical-paths, CTM/CTS, power estimation, DFM, LEC and fullchip timing.
- KNC -- Backend integration (floor-planning to metal fill) of 3 top level analog/digital *Megablocks* namely *LDIO, LDIOPLL and LPCPLL*. The first is an IO block and the others are analog PLL's. Managed block/chip level static timing analysis (STA) using Synopsis DC and ICC tools. Used frontend/physical Universal Power Format (UPF) based synthesis to do signal and power floor-planning of 5 local and top-level supplies. Completed CTS of 1.6 Ghz core clock and 100 Mhz test clocks routes. Manually pre-routed critical clocks. Completed LEC and fullchip noise analysis.
- UPF Low Power -- Pioneered Synopsis's Power Aware UPF and Powerintent based tools to place and route an I/O and PLL blocks with embedded regulators. This allowed RTL to be free of all power definitions. It also eliminated manual level-shifter insertion between power domains by auto placing them. Five power domains including regulated and switched ones were automatically floor-planned by this method.

Consultant. Austin Silicon, Austin, TX   2001-2008

Design Engineering

- *Intrinsity Incorporated. Austin, TX***:** Magma Blastfusion based design of TSMC 90nm Jtag TAP Controller, MBIST Jtag interface, On Chip Debug (ocd) Jtag 2.5 Ghz interface, 2 GHz 64 bit timer, 32 bit Decrementer/Timebase unit. Delivered RTL, Synthesis, Floorplan, and Pathmill timing analysis. Created 2.5 Ghz standard cell library "Volcanos" used to redesign slow blocks in the ARM core. Power analysis of the revised ARM core

- *Intel Corporation. Chandler, AZ*: Migrated Xscale core Manzano from 130nm to 65nm. Fixed edge rates, speed paths, SI, LEC, architectural verification using Intel's pattern matching tools. Pathmill timing of domino designs, ERC and LVS.

- *Coherent Logix. Austin, TX*: Full chip timing, gate sim, synthesis setup, area array C4 IO/ESD designs, power management unit and padring of the HyperX processor. This is an arrayed processor containing 15M transistors meant for Hyper Spectral applications. Cadence RC, FE, Modelsim and Debussy.

- Design of 1.8v EIA-644 LVDS IO driver and differential receiver with shutdown. The receiver has 100mv sensitivity over the entire 1.8v CMR. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. Sectioned padring switch off with hardware/software wakeup. Designed the pad driver for the 1.8v SSTL_18 outputs.

- *Advanced Micro Devices. Austin, TX*: *Designed* a pcix2.0 533 mbits/s IO. This IO is one of a kind and handles all pcix specs namely 33, 66, 133, 266 and 533 mbits/s. PrimeTime, Starsim simulations of all 64 IO bits. Delivered Technical Analysis Report. Part is used in Opteron interfaced to a hyper transport bus.

  Designed the above cell using proprietary slew rate control using 130nm UMC process with 1.2V supply for core and 3.3V and 1.5V for the output buffers (mode 1 and 2 respectively). This is a non-analog easily scalable design.

  Patent (proposed): Process Switchable Low Noise Output Buffer.

- *Mathstar Incorporated. Dallas, TX*: Spice-designed clock-tree, analyzed speed-path circuits and created library cells for a 1Ghz networking chip called the Field Programmable Object Array Processor. Design used hex shaped processors array together that communicated 6-ways.

- *Silicon Metrics/Magma Design. Austin, TX*: Designed the EDA tool SiliconSmartIO. This flagship product is used to certify IO's. The tool also does padring analysis and reports design flaws. It's capable of compliance testing LVDS, USB, I2C, I2S and SDRAM Interface by using Spice analysis customized for each ieee spec. The product made cover of Electronic Design. Deliverables included: a) Textually modeling the specs b) Spice decks for each model c) Methods of signal measurements to verify compliance d) Interface to the EDA tool SiliconSmart Cellrator used to generate static timing files and .LIB e) Graphical display of compliance f) Help with technical publications and press release g) Product licensing of modules, h) Customer support, and EIA certification.

Intel Corporation. Austin, TX   Previous Tenure

Design Engineer: StrongArm, Xscale, Tejas Desktop Platform Group (DPG)

- Tejas 64bit 7GHz library cells. Low Noise 50ps FF, CSA, 72 bit adders, 30ps Zero Detects. Verilog model, Static Timing analysis, .LIB, Noise Analysis tests.

- ARM Core. Virtuoso Floorplanning with power management. Circuit design of ESD, Padring, USB driver circuit, programmable IO buffer circuit for 600 MHz 0.25W Xscale Cotulla. Pad-Package mapping, package substrate design provided to NGK for manufacture, power based pin ordering, tests for 75uA Sleep and Drowsy Modes. Simulation of 256 pad cells in Verilog/VHDL, test fixture, IO/Analog .lib, padring STA, IBIS board driver model.

- SDRAM IO drivers circuit for 0.5 watt StrongArm SA1110. Designed Sleep Mode circuit that switches off core and padring under powersave conditions. Wrote Verilog models for the IO cells and Jtag and ran Regression tests. Developed and modeled design rules for boards and created IBIS models. Attended Synopsis Black-Box Timing Model training.

Awards: Intel - Leaping Lizard Award for Excellent Contribution

Defensive Publications: Motorola - Preventing False Latching in VLSI Circuits.

Patents: AMD - A Supply Bounce Controlled Output Buffer.

         Intel - A Low Leakage Level Translator

            USB Cable Disconnect Detect

            Driver Z-Match output buffer

            Regulator Independent IO Sleep Controller

Education

MSEE	University of Texas at Austin	Austin, TX
MSc (Atomic and Molecular Physics)	University of Karachi	Karachi, Pakistan
BSc (Physics)	University of Karachi	Karachi, Pakistan

Interests

Electromigration in powergrids and low power technologies.