

# Zahid Ahsanullah

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## Objective

Consultant for Circuit Design, Verification, IO/ESD/Padring Designs and other VLSI related work.

## Education

1985	MSEE	University of Texas At Austin	Austin, TX
1981	MSc Physics	University of Karachi	Karachi, PK
1979	BSc Physics	University of Karachi	Karachi, PK

## Extract

My design experience is varied and ranges from full custom to RTL and Synthesized designs. I have worked on large processors like Intel's 64 bit 8 Ghz Tejas, Motorola 68040, and AMD 29K. I am also experienced in low power DSP chips used in Handhelds. Many of my years have been spent doing Mixed Signal IO and ESD design for which I have received patents listed below. I can code RTL in both Verilog and VHDL, and have setup synthesis environments for Magma Blastfusion, Cadence First Encounter and Synopsis Design Compiler tools. I have good Post Silicon Debug experience and a somewhat outdated SCAN experience. I have consulted for several years with some well known Design and EDA firms and designed my own IP; a PCIX 2.0 32 bit IO that runs at the new 533 Mb/s spec. I am currently employed as a full time Analog Integration Engineer at Intel for the next generation [Larrabee](#) Graphics Processor. My resume below lists my experience as a [consultant](#) and as a [regular employee](#).

## Experience Consulting

2001-2008 Austin Silicon Incorporated Austin, TX

### Principal.

[Austin Silicon](#) is the firm through which I consult. It has operated for 8 years and provided technology support to several companies in Austin and around US. The following lists the services provided:

**Intrinsity Inc. 2007-2008 - Design and Verification Consultant:** Designed a 10 Mhz Jtag Tap Access Port Controller, the Memory Bist (mbist) Jtag interface and the On Chip Debug (ocd) Jtag interface. The block allows the jtag unit to configure and control the mbist and ocd units and capture and synchronize 2.5 Ghz bist data on the fly during runtime. The completed package included the RTL, Synthesis, Floorplanned layout, Pathmill timing analysis, tcl scripts and design documentation. Magma Blast Synthesis tools were used throughout including floorplan.

Designed a 2 GHz 64 bit timer, 32 bit decremter and timebase unit. Delivered RTL, floorplan, STA, Magma scripts and integration document.

Created and maintained existing and new 2.5 Ghz standard cell library volcanos using Magma Blastfusion tools. Created library components for custom cells which were then embedded in an ARM core as replacements for slower blocks. Wrote tcl scripts for running synthesis, floorplan and power domain analysis of the ARM core with these new cells.

**Intel Chandler 2006 (Feb-Jul) - Circuit Consultant:** Hired as a consultant to help with migrating the Xscale core named Manzano from 130nm to 65nm. I was given the task of carrying out circuit fixes related to signal edge rates, speed paths, signal integrity, logic equivalency tests using LEC as well as architectural verification runs using Intel's own pattern matching tools. Pathmill timing analysis tool was used to analyze and fix problems with domino and other non-standard designs. Layout changes were verified by me both visually and using erc and lvs. All tasks were completed in a timely manner and delivered to the team.

**Coherent Logix 2005-2006 - Circuits and Verification:** Completed full chip timing analysis, synthesis methodology, IO/ESD designs, Power Management architecture and Padring layout supervision of the HyperX processor. This is a large network based arrayed processor containing 15M transistors meant for Hyper Spectral applications. The IO's were area array type using C4 bumps.

Conducted full chip timing analysis on an extracted netlist customized for this purpose. The analysis was carried out using Cadence's RC and First Encounter tools.

Developed the RC synthesis scripts for the team. The script has been successfully used to synthesize varied designs within the chip and uses methods to ensure proper interface timing between the arrayed processors. Both Synopsis and Cadence's tools can use the scripts.

Assisted with full chip gate simulation efforts using Modelsim and Debussy.

Designed a 1.8v EIA-644 LVDS IO driver and differential receiver with a low power shutdown mode. The receiver has 100mv sensitivity over the entire 1.8v range. This is a part of a complex IO cell that can switch from being an LVDS cell to SSTL, LVTTL or GPIO just by flipping some bits. The ESD design is based on IBM's RC clamps and diode models available for the CMOS8RF 130nm process. The Padring is capable of being switched off in sections with an external or software Wakeup feature. Designed the driver for the 1.8v SSTL\_18 outputs.

**AMD 2004 - Circuit Consultant:** Helped design an analog pcix2.0 IO to run at the new 533 mbits/s spec. This IO is the only running kind in the industry and can handle all previous pcix specs namely 33, 66, 133, 266 and 533 mbits/s. Also delivered with the product PrimeTime timing files, Starsim simulations of all 64 data and control io's and Technical Analysis Report. The part is for the Opteron interfacing to a hyper transport bus.

**Austin Silicon 2004 - IP Development:** Designed a proprietary IP of the above-mentioned pcix2.0 using non-analog techniques around my as yet unregistered patent on slew rate control. The design uses a 130nm UMC process using 1.2V supply for core and 3.3V and 1.5V for the output buffers (mode 1 and 2 respectively). This is a non-analog design so it is easily scalable.

**Patent** (in progress): Process Switchable Low Noise Output Buffer.

**Mathstar 2003 - Design Consultant:** Designed a 1Ghz Field Programmable Object Array Processor hexagonal in shape to allow for a 6-way communication between independent neighboring processors. The chip has networking application and the following were delivered: Modeling of the critical data path of the architecture in Spice to confirm 1Ghz speed. Designed components of the 1Ghz standard cell library that included circuit design, verilog gate and functional models, and PrimeTime files. Assisted with Clock Tree design, and layout floor plan of the interconnected processors.

**Siliconmetrics (now Magma) 2002 – EDA Consultant:** Designed the EDA tool [SiliconSmartIO](#). This was a flagship product meant to certify and design specialized as well as standard IO's. The tool also does Padring analysis and offers insight into design flaws. The capability includes compliance testing LVDS, USB, I2C, I2S and SDRAM Interface by using Spice analysis customized for each specification. The product was on the cover of [Electronic Design](#) in August 2002. Deliverables included: a) A textual description of modeling issues implied by the specs b) Spice decks for each model c) Methods of signal measurements to verify compliance to published specs d) Interface to the EDA tool SiliconSmart Cellrator used to generate static timing files and .LIB e) Graphical display of compliance f) Help with technical publications and press release g) Licensing of product slew, h) Marketing, customer visits, and EIA certification.

**Experience  
Employed**

2008-Present Intel Corporation Austin, TX

**Integration Engineer: Larrabee Processor, Visual Computing Group (VCG)**

Currently helping out with tapeout efforts related to the Larrabee-1 processor. My responsibilities include doing verification runs which include running rc extractions, lvs, etc, noise analysis, formal verification, audit runs and other tools. For Larrabee-2 I will be responsible for full chip synthesis, timing, and design integration of all analog and digital blocks for final verification and analysis.

1998-2001 Intel Corporation Austin, TX

**Design Engineer: StrongArm, Xscale, Tejas Desktop Platform Group (DPG)**

Responsibilities included low power ARM based core design, IO design and 7 Ghz library cell development.

Developed 7GHz library cells for DPG's 64bit processor. Examples are Low Noise 50ps CK-Q FF, CSA, Fast 72 bit adders, 30ps Zero Detects. This also includes Verilog model for the cells, Static Timing analysis, .LIB files, Noise Analysis tests and layout in two different aspect ratios.

Designed ESD, Padring, USB and a Low Noise Programmable IO buffer for the 600 MHz, 0.25W Xscale part called Cotulla. Created Pad-Package mapping files, Package Substrate design, Package Pinorder file, tests for 0.25W operation and tests for 75uA Sleep and Drowsy Modes. These modes along with Power Island circuits are innovations for low power. For verification I modeled 256 pad cells in VHDL, wrote a test fixture for the Padring and ran VHDL simulations. Hand created .LIB timing files for the IO Cells including the analog ones, and ran static timing analysis on the RC extracted Padring. Created IBIS models for the drivers as well as board models for various applications.

Designed the SDRAM memory interface IO buffers for the half watt StrongArm SA1110. The design incorporates a Sleep Mode that switches off some supplies to core and Padring under Powersave conditions. Wrote Verilog models for the IO cells and Jtag and ran Regression tests. Developed and modeled design rules for boards and created IBIS models. Attended Synopsis Black-Box Timing Model class.

**Patents Accepted:** A Low Leakage Level Translator, USB Cable Disconnect Detect, Driver Z-Match output buffer, Regulator Independent IO Sleep Controller.

**Award:** Leaping Lizard Award For Excellent Contribution.

1992–1998 Motorola Incorporated Oakhill, TX

**Staff Engineer: General DSP Parts, DSP MC56000 family of products and MC68040 High End Processor**

Responsibilities for 56000 included doing parts of the Core, the Bus Interface Unit (BIU), IO, Padring and ESD. For the 68040, Verilog models for the core blocks, SCAN and DFT lead, silicon debug, verilog verification of all bug fixes and full chip logic simulations.

Designed a 3X, 40 MHz, Full Digital PLL for the low power EFRSMoC. This DSP chip was used in Startac cellular phones. Mentor ModelSim was used for Verification and estimating Lock Time.

Migrated a 50k Dual Port SRAM from 180nm UDR to 130nm CDR process with associated verilog descriptions.

Designed a 40 MHz programmable IO for the 16-bit DSP chip MC56824. The circuit used an invented slew-rate control circuit, dual buffer operation and some innovative noise control designs. Also included in the design were jtag cells and control unit, padring behavioral model and test fixture, .LIB files and IBIS models.

Designed the IO, Jtag and the Bus Interface Unit (BIU) for the MC56800 DSP family. The BIU control unit was synthesized from an RTL using Synopsis Design Compiler and Verilog, PrimeTime, Timemill and Pathmill were used for verification. The IO was a low power, low noise programmable Dual Buffer design using a proprietary edge rate control circuits.

DFT lead for the 68040 test group. My responsibilities were to hand insert Scan Chains, generate new tests and pattern files and deliver production scan pattern files. Pattern verification runs were carried out in verilog.

Worked in the MC qualifying team for the XC68040. Our objective was to MC qualify the part by fixing circuit bugs. We created looping test patterns, Ebeam probes, FIB fix, new circuit spice simulation and finally verilog confirmation of old and new design for sameness. Our team fixed more than one thousand circuit bugs this way to achieve 6-Sigma qualification.

**Defensive Publication:** Preventing False Latching In VLSI Circuits.

1984–1992 Advanced Micro Devices Austin, TX

**Senior Design Engineer: Am29000 RISC Processor Family and other products**

Responsibilities included writing Verilog code for the 29k and 29050 custom blocks and creating their circuits. Carrying out architectural verification runs with customized behavioral codes. Finally layout verification using LVS, ERC and DRC.

Custom designed the circuits for the Processor Bus Control Unit, Memory Bus-Watch state machine and Processor-Memory-Access state machine for the 32bit Am29060 Integrated Cache Unit. Wrote Verilog behavioral for the above.

Custom designed the circuit of the Special Register Block and the Load-Store section of a Supersaclar RISC processor companion to the 29000 families. Wrote behavioral in verilog and tested it in full chip runs.

Designed patented the Color Burst Memory Interface IO buffer for the Am290XX series RISC Processors.

**Patent Accepted:** A Supply Bounce Controlled Output Buffer.

**Other**

Focused Ion Beam (FIB) debug, EBEAM and Microprobing, analog and digital board design.